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ECE4304- Lab 5

3/17/2021

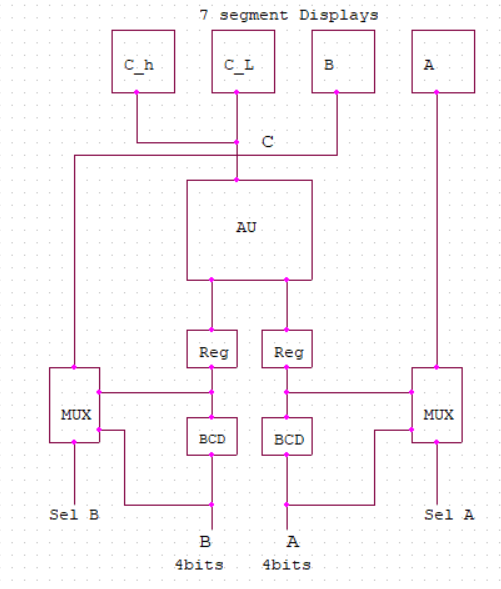
Professor M. Aly

AU Implementation in VHDL

**Purpose:**

1. Design an Arithmetic unit that could perform adding, multiplying, subtraction, and division.
2. The two inputs are 4 bits each and should be displayed in hex and BCD on the 7segment displays based on the select signals.
3. The result is displayed on the displays as A, B and C(low and high).
4. All possible corner cases was defined using a testbench textio.

**Procedure:**

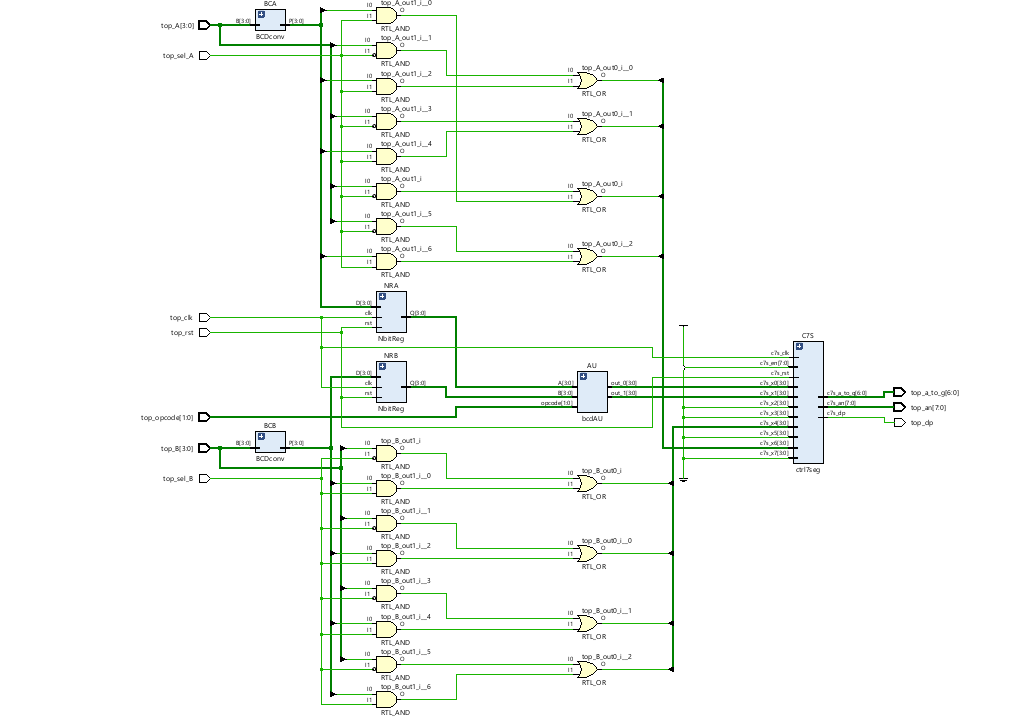
 The following components were created:

1. BCD converter for input A
2. BCD converter for input B.
3. Tow N bit registers to save the values of the binary and the BCD input value for A and B.
4. Multiplexers to select between the binary and the BCD values that needed to display.
5. AU component to perform all the operations needed.
6. 7segment unit.

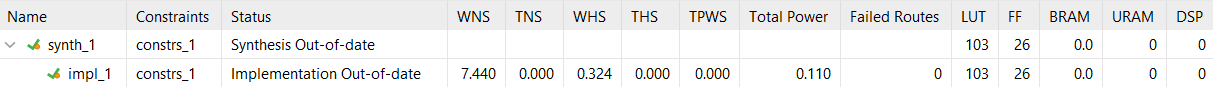
Top entity to wrap all the component together and create the desired design.

**Schematic:**

Wrapping all the component created, we end up having the following design:



**Power and Resources Used:**



103 lookup tables and 0.110 total power used to implement this design using Vivado.

**Difficulties:**

Difficulties in implementing the division and the 10’s complement for the subtraction operation.

**Work Contribution:**

* We had a meeting to brainstorm and explain the main idea of the lab, and we created the schematic so that everyone would work individually to achieve the most optimized design.
* We had a zoom meeting to choose the design with less power consuming, then we were able to demo our implemented design and cover all the corner cases.
* Documentation and reports were evenly distributed, and it covered all the steps of our successfully implemented design.